Amendments to the Claims

Listing of Claims:

Claim 1 (Currently Amended): A high-to-low level shifter being coupled to a first voltage and a second voltage, wherein the first voltage is larger than the second voltage, the high-to-low level shifter comprising:

an inverter for receiving an input signal and generating an inverse input signal, wherein the inverter operates at the first voltage; and

a level shifter for generating an output signal according to the input signal and the inverse input signal, the level shifter comprising a pull-up unit for receiving the input signal and a pull-down unit for receiving the inverse input signal, wherein the level shifter operates at the second voltage, the logic level of the output signal corresponds to the second voltage, [[and]] the logic value of the output signal corresponds to the input signal, and the pull-up unit and the pull-down unit are coupled to the output signal.

Claim 2-4 (Cancelled)

Claim 5 (Currently Amended): The high-to-low level shifter of claim [[2]] 1, wherein the pull-up unit is an NMOS transistor.

Claim 6 (Currently Amended): The high-to-low level shifter of claim [[2]] 1, wherein the pull-down unit is an NMOS transistor.

Claim 7 (Currently Amended): The high-to-low level shifter of claim [[2]] 1, wherein both the pull-up unit and the pull-down unit are high voltage devices.

Claim 8 (Original): The high-to-low level shifter of claim 1, wherein the level shifter is

set inside an integrated circuit.

Claim 9 (Original): The high-to-low level shifter of claim 1, wherein the inverter is set outside an integrated circuit.

Claim 10 (Original): A high-to-low level shifter comprising:

a first transistor for receiving a first input signal; and

a second transistor for receiving a second input signal which is the inverse of the first input signal, wherein the first transistor and the second transistor are coupled to an output end for outputting an output signal, the logic value of the output signal corresponds to the first input signal and the second input signal;

wherein the logic level of the first input signal and the second input signal correspond to a first voltage, the logic level of the output signal corresponds to a second voltage, and the first voltage is larger than the second voltage.

Claim 11 (Original): The high-to-low level shifter of claim 10, wherein both the first transistor and the second transistor are NMOS transistors.

Claim 12 (Original): The high-to-low level shifter of claim 10, wherein the first transistor and the second transistor operate at the second voltage.

Claim 13 (Original): The high-to-low level shifter of claim 10, wherein the first transistor is coupled to the second voltage.

Claim 14 (Original): The high-to-low level shifter of claim 10, wherein the high-to-low level shifter is set inside an integrated circuit.

Claim 15 (Original): The high-to-low level shifter of claim 10, wherein the first

voltage is 3.3V.

Claim 16 (Original): The high-to-low level shifter of claim 10, wherein the second voltage is less than 0.9V.

Claim 17 (New): A high-to-low level shifter being coupled to a first voltage and a second voltage, wherein the first voltage is larger than the second voltage, the high-to-low level shifter comprising:

an inverter for receiving an input signal and generating an inverse input signal, wherein the inverter operates at the first voltage; and

a level shifter for generating an output signal according to the input signal and the inverse input signal, the level shifter comprising a pull-up unit and a pull-down unit, wherein the level shifter operates at the second voltage, the logic level of the output signal corresponds to the second voltage, the logic value of the output signal corresponds to the input signal, and both the pull-up unit and the pull-down unit are high voltage devices.

Claim 18 (New): The high-to-low level shifter of claim 17, wherein the pull-up unit is for receiving the input signal, the pull-down unit is for receiving the inverse input signal, and the pull-up unit and the pull-down unit are coupled to the output signal.

Claim 19 (New): The high-to-low level shifter of claim 17, wherein the pull-up unit is for receiving the inverse input signal, the pull-down unit is for receiving the input signal, and the pull-up unit and the pull-down unit are coupled to the output signal.

Claim 20 (New): The high-to-low level shifter of claim 17, wherein the pull-up unit is an NMOS transistor.

Claim 21 (New): The high-to-low level shifter of claim 17, wherein the pull-down unit is an NMOS transistor.

Claim 22 (New): The high-to-low level shifter of claim 17, wherein the level shifter is set inside an integrated circuit.

Claim 23 (New): The high-to-low level shifter of claim 17, wherein the inverter is set outside an integrated circuit.

Claim 24 (New): A high-to-low level shifter being coupled to a first voltage and a second voltage, wherein the first voltage is larger than the second voltage, the high-to-low level shifter comprising:

an inverter for receiving an input signal and generating an inverse input signal, wherein the inverter operates at the first voltage, and the inverter is set outside an integrated circuit; and

a level shifter for generating an output signal according to the input signal and the inverse input signal, wherein the level shifter operates at the second voltage, the logic level of the output signal corresponds to the second voltage, and the logic value of the output signal corresponds to the input signal.

Claim 25 (New): The high-to-low level shifter of claim 24, wherein the level shifter comprises a pull-up unit and a pull-down unit.

Claim 26 (New): The high-to-low level shifter of claim 25, wherein the pull-up unit is for receiving the input signal, the pull-down unit is for receiving the inverse input signal, and the pull-up unit and the pull-down unit are coupled to the output signal.

Claim 27 (New): The high-to-low level shifter of claim 25, wherein the pull-up unit is

for receiving the inverse input signal, the pull-down unit is for receiving the input signal, and the pull-up unit and the pull-down unit are coupled to the output signal.

Claim 28 (New): The high-to-low level shifter of claim 25, wherein the pull-up unit is an NMOS transistor.

Claim 29 (New): The high-to-low level shifter of claim 25, wherein the pull-down unit is an NMOS transistor.

Claim 30 (New): The high-to-low level shifter of claim 25 wherein both the pull-up unit and the pull-down unit are high voltage devices.

Claim 31 (New): The high-to-low level shifter of claim 24, wherein the level shifter is set inside an integrated circuit.